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(71) Applicant: RICOH CO LTD

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(54) NOVOLATILE SEMICONDUCTOR MEMORY DEVICE

(57) Abstract:

PURPOSE: To restrict the charge gain by employing an insulation film having low thermal hysteresis of stress as a passivation film.

CONSTITUTION: A source region 4, a drain region 6 and a floating gate electrode 10 are formed on a silicon substrate 2 and an ONO dielectric film 12, comprising first and third silicon oxide layers and a second silicon nitride layer, is deposited thereon. A first layer metallization 18 is then connected with the source region 4 and the drain region 6 through a contact hole made through an insulation film 16 formed on a control gate electrode 14. Subsequently, a second layer metallization 22 is formed on an interlayer insulation film 20 and connected with the metallization 18 through a through hole. The charge gain can be restricted by employing a TEO silicon oxide/silicon nitride and TEO silicon oxide having low thermal hysteresis of stress, respectively, as a passivation film 24 on the metallization 22 and the interlayer insulation film 20.

Abstract Drawing